[3] B. S. Siegal, "Schottky diodes–where we stand today," *Microwaves*, vol. 10, pp. 44–46, Apr. 1971.
[4] R. O. Wright, "The backward diode–when and how to use it," *Microwaves*, vol. 3, pp. 22–27, Dec. 1964.
[5] —, "New twist for backward diode help from low-noise amplifier," *Electronics*, vol. 39, pp. 74–77, July 11, 1966.
[6] M. E. Brodwin, C. M. Johnson, and W. M. Waters, "Low level synchronous mixing," in *IRE Nat. Conv. Rec.*, vol. 1, pt. 10, pp. 52–57, Mar. 1953.
[7] G. W. C. Mathers, "Homodyne generator and detection system," in *IRE Wescon Conv. Rec.*, vol. 1, pt. 1, pp. 194–200, 1957.
[8] J. H. Richmond, "Measurement of time-quadrature components of microwave signals," *IRE Trans. Microwave Theory Tech.*, vol. MTT-3, pp. 13–15, Apr. 1955.
[9] B. B. O'Brien, "A pseudo-superheterodyne receiver for measuring phase and amplitude," *IEEE Trans. Instrum. Meas.*, vol. IM-16, pp. 124–128, June 1967.
[10] G. E. Schafer, "A modulated subcarrier technique of measuring microwave phase shifts," *IRE Trans. Instrum.*, vol. I-9, pp. 217–219, Sept. 1960.
[11] R. J. King, "Real time measurement of microwave parameters and EM fields," *IEEE Trans. Instrum. Meas.*, vol. IM-21, pp. 2–10, Feb. 1972.
[12] B. A. Howarth and T. J. F. Pavlásek, "Analysis of automatic homodyne method amplitude and phase measurements," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-20, pp. 623–626, Sept. 1972.
[13] G. E. Schafer and R. R. Bowman, "A modulated sub-carrier technique of measuring microwave attenuation," *Proc. Inst. Elec. Eng.*, vol. 109B(23), pp. 783–786, May 1962.
[14] W. E. Little, "Further analysis of the modulated subcarrier technique of attenuation measurement," *IEEE Trans. Instrum. Meas.*, vol. IM-13, pp. 71–76, June-Sept. 1964.
[15] H. C. Torrey and C. A. Whitmer, *Crystal Rectifiers*. New York: McGraw-Hill, 1948.
[16] G. C. Messenger and C. T. McCoy, "Theory and operation of crystal diodes as mixers," *Proc. IRE*, vol. 45, pp. 1269–1283, Sept. 1957.
[17] S. T. Eng, "Low-noise properties of microwave backward diodes," *IRE Trans. Microwave Theory Tech.*, vol. MTT-9, pp. 419–425, 1961.

Automatic Test System for an Analog Computer

J. FRANK ROSS, DOUGLAS G. PINCOCK, MEMBER, IEEE, ROBERT J. KAVANAGH, AND DAVID M. WANAMAKER

Abstract—**This paper describes the design, construction, and performance of an automatic test system for the analog portion of a hybrid computation system. The system, which is capable of carrying out complete dynamic testing of each analog component, uses the digital portion of the hybrid system to provide the desired control with the result that the requirement for sophisticated stimulation and measurement equipment is minimized. The hardware and software of the system are both modular in nature in order to provide versatility and to facilitate modifications and additions as required. The design philosophy is such that the methods used are not limited to a particular analog computer. In fact, they have applications in the testing of many types of electronic equipment.**

I. Introduction

ONE OF THE MAIN difficulties in making efficient use of hybrid computation systems is the fact that failures in the analog subsystem are relatively frequent. It is, of course, important that such failures be isolated before they introduce errors into solutions. This can be accomplished to a certain extent through extensive use of static checks by programmers [1], [2]. These checks, however, provide no guarantee that components are operative in a dynamic sense, i.e., that integrators do in fact integrate, that nonlinear function generators work in all quadrants, that the frequency response of amplifiers is adequate, etc. Therefore, if users are to have confidence in a hybrid system, it is essential that frequent preventative maintenance tests be carried out on all components. Unfortunately, such tests tend to be very time consuming and hence, are carried out relatively infrequently. Due to the presence of a general-purpose digital computer in the hybrid configuration, it seems natural to investigate the use of automatic testing as a solution to this problem. This paper describes the development of an automatic test system for the analog portion of the EAI 590 Hybrid Computation system at the University of New Brunswick, Fredericton, N.B., Canada.

One of the main considerations in the design of the automatic test system was to minimize costs by using the digital computer as much as possible in place of sophisticated stimulation and measurement equipment. In addition, both hardware and software were designed to be modular in nature in order to provide versatility and facilitate modifications and additions as required.

II. Overview of the Test System

Stuehler [3] divides any general automatic test system into the following logical units, as shown in Fig. 1:

1) a unit which is under test (UUT);

Manuscript received April 30, 1973; revised July 18, 1973. This work was supported by the National Research Council of Canada under Grant A5155. This paper was presented at the 1973 Electrical and Electronic Measurement and Test Instrument Conference (EEMTIC), Ottawa, Ont., Canada, May 15–17.

J. F. Ross is with the Defense Research Establishment Valcartier, Defense Research Board, Valcartier, P.Q., Canada.
D. G. Pincock, R. J. Kavanagh, and D. M. Wanamaker are with the Electrical Engineering Department, University of New Brunswick, Fredericton, N.B., Canada.

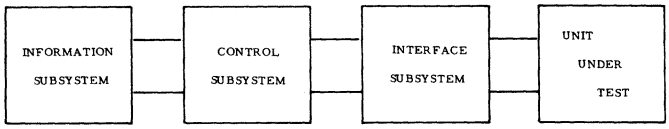

Fig. 1. Basic test system components.

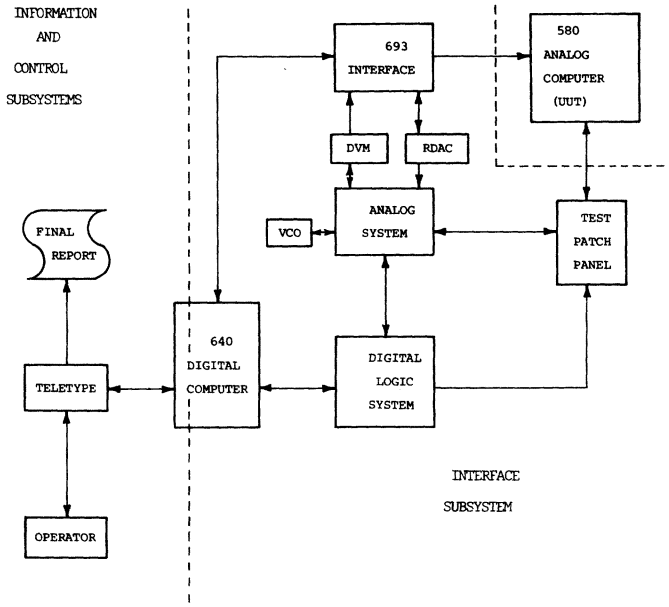

Fig. 2. Automatic test system.

2) an interface subsystem which connects to the unit under test, provides environment and stimuli, and detects and measures responses;
3) a control subsystem which commands the interface subsystem, receives converted responses and makes decisions as to subsequent stimuli and environmental conditions;
4) an information subsystem which provides the control subsystem with data describing the UUT, specified test features and sequences, provides analysis to determine if the UUT is good or bad, reports test results to the operator, and records the test results.

In the EAI 580 analog-computer test system, the information subsystem is required to process large amounts of data. Accuracy and repeatability of tests and flexibility in methods of analysis are important. For these reasons, a software implementation was chosen for this subsystem.

One of the prime requirements of the control subsystem is versatility, and therefore, software was used for this purpose. Software here also provides a very useful man-machine interface, allowing conversation (via a keyboard/printer) between the system and operator, as opposed to the inevitable lights, switches, dials, and buzzers required by hardware control subsystems.

Although the interface subsystem may often be partially implemented by software (signal processing such as filtering, integration, and differentiation), this particular application ruled out software except for counting and timing purposes.

Fig. 2 shows the general hardware organization of the system. The following description of a typical test sequence is intended to give the reader an idea as to how the different system components interact as well as to relate the organization to that shown in Fig. 1. In a typical test sequence the operator enters information at the keyboard concerning the components to be tested, type of test, and type of printout desired. The purpose of the control subsystem is to provide a sequence of commands which the digital logic uses to control the rest of the interface subsystem hardware. This sequence of commands causes first the selection and configuration of the unit under test through control of switches on a special purpose automatic patch panel, and then the application of appropriate test signals and the measurement of appropriate responses through the analog system. The information program receives all test results, performs format conversion and error checking, and finally prints the test results.

The hardware for the system was designed to allow complete flexibility in the type of test which could be carried out. In the following sections the important features of each hardware subsystem are described.

III. Patch Panel System

Configuration Control

A fully expanded EAI 580 analog computer contains 64 high-gain chopper stabilized operational amplifiers. In order to test the basic functioning and frequency response characteristics, it is necessary to connect each amplifier as a unity-gain inverting summer. Once this is done, the amplifier can subsequently be used as a multiplier, integrator, or other circuit so that each computing network adjacent to an amplifier can be tested. Thus the automatic patch panel must be capable of connecting each amplifier into one of two possible configurations–one for summers and the other for alternates. The patch panel was designed so that all amplifiers change configuration simultaneously, utilizing a total of 206 switches.

Output Select System

There are 64 amplifiers and eight comparators whose outputs must be selected for measurement. This is accomplished by switching the desired output onto an external response bus on the patch panel (bus 3), using a total of 72 switches. The control of these switches was designed so that it would not be possible for more than one switch to be closed at any one time. Otherwise, two or more active outputs would be connected together through bus 3.

Only tests of a dc nature were foreseen for potentiometers and therefore, the internal 580 low-frequency selection system is utilized for these tests.

During amplifier balance tests, the 580 internal selection system connects the output of the selected amplifier stabilizer section to the 580 stabilizer bus. This signal is then routed directly to the analog measuring system without the requirement for any patch panel connections.

Input Select System

In order to test a given component, certain stimulus signals have to be applied to the component inputs. For some components, notably the multipliers, two input signals are required simultaneously and, therefore, component inputs can be con-

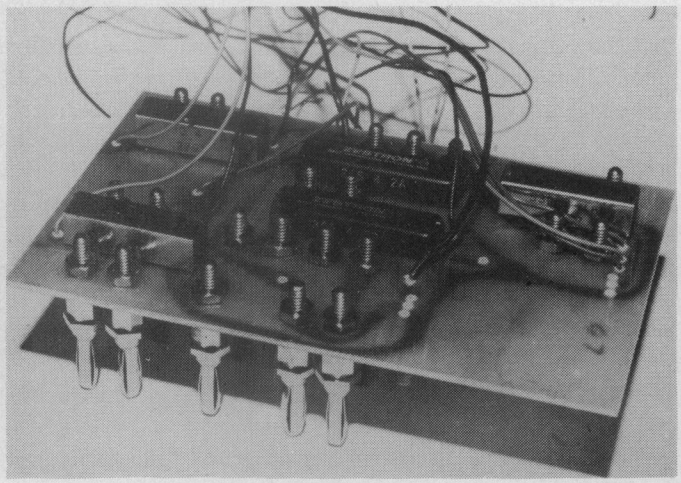

Fig. 3. Typical test module.

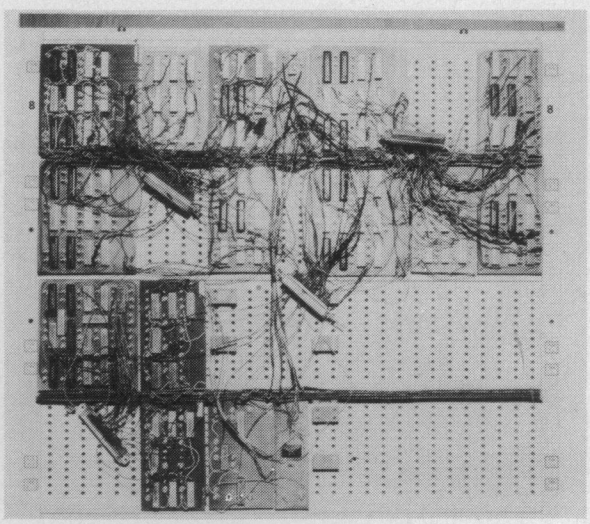

Fig. 4. Patch panel with cover removed.

nected to either of two-patch-panel stimulus buses (bus 1 and bus 2) as required. If each input were switched independently, a total of 134 switches would be required. However, by combining inputs in parallel (e.g., all four summer inputs on a quad amplifier module), a reduction by a factor of two in the number of switches was obtained along with convenience and simplified testing.

Control Lines

To enable the logic system to select a component for testing and to define its configuration and operational mode, a number of control lines are required for the operation of the patch panel. These lines can be grouped as follows:

1) the two configuration control buses I and II, which are used to activate the two groups of switches to select such configuration;
2) a total of 72 output select control lines to control the 72 output selection switches;
3) a total of 80-input select control lines; and
4) an additional 24 control lines to control track/store modes and D/A switch states.

Construction

Reed relays, driven directly from digital logic circuits, were used for all switches in the system since they were the only type of switch that satisfied the requirements of low on resistance, low leakage when off, and low cost [4]. To mount the relays on the patch panel and make necessary connections to patch panel holes, test modules were constructed as shown in Fig. 3. The main part of each module is a circuit board on which the relays are mounted. Standard banana plugs were used to provide both the mechanical mounting and the electrical contacts to the patch panel holes, and hence to the components. The prime consideration here was to mount each relay as close as possible to the points it was required to connect, in order to minimize stray wiring capacitances.

The patch panel system is divided logically into 24 test modules of six basic types. Each module is completely independent and can be removed for checking or repair without affecting the rest of the system. Each module is attached to six bus lines on the panel which are two stimulus buses (bus 1 and bus 2), one response bus (bus 3), two configuration select buses, and one 5-V relay supply bus.

Fig. 4 is a photograph of the patch panel system. As the analog computer is expanded further, test modules will be added. In order to take the photograph it was necessary to remove the patch panel cover. The 50 pin connectors, which make connection to the digital logic system would normally mount on this cover.

IV. Analog System

Fig. 5 shows the general organization of the analog system. All of the connections shown are made by logical control of reed relays. The analog circuitry was constructed on two plug-in cards and is mounted in an equipment chasis along with the digital logic.

Stimulus System

Stimulus signals are obtained from the 580 reference digital-analog converter (RDAC) (variable dc) or a voltage controlled oscillator (VCO) (ac). The RDAC can set any voltage from 0 to 9.999 V with a 1 mV resolution, and the VCO (which is controlled by the RDAC) provides 20-V peak-to-peak ac signals at frequencies from 1–500 kHz. Neither of the previous sources is capable of driving low-impedance loads and, therefore, inverting and noninverting unity gain buffers are provided which can deliver up to 20 mA. Although the buffer outputs roll off above 100 kHz, no inaccuracies are introduced into frequency response tests since both input and output amplitudes are measured.

In addition to these two main stimulus sources, both stimulus buses can be independently connected to the analog computer +10-V reference, −10-V reference, or ground.

Measurement System

Fig. 6 shows a simplified schematic of the peak detector. The circuit can be set up via switches to read either the positive or negative peak of the input ac signal. For positive peaks, it functions as follows.

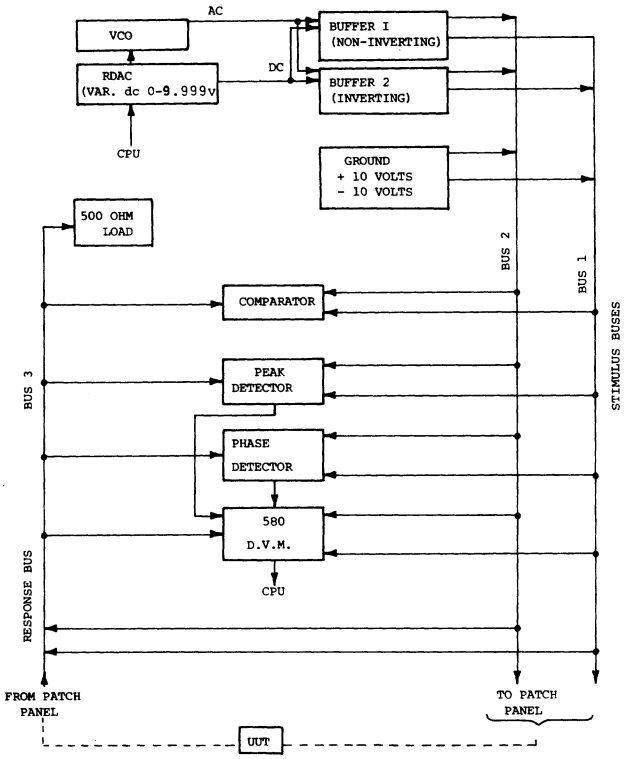

Fig. 5. Analog system.

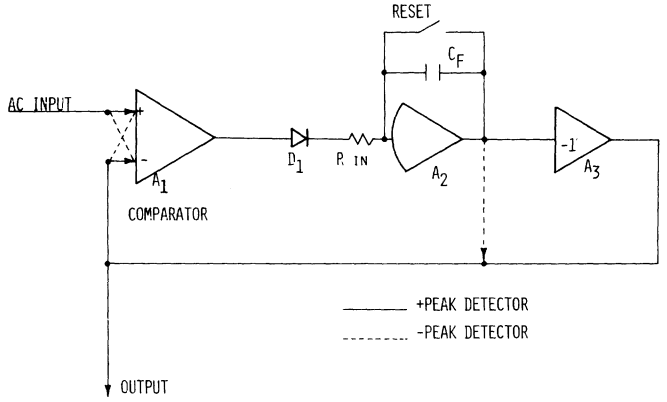

Fig. 6. Simplified peak detector system.

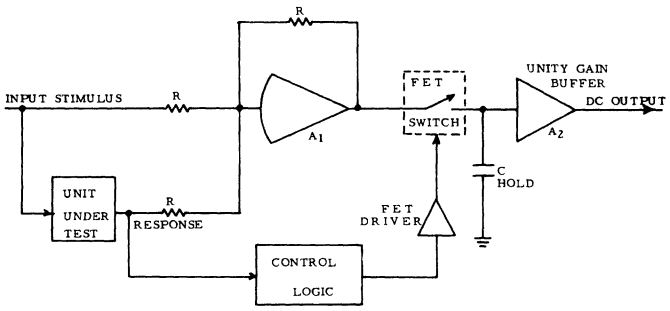

Fig. 7. Simplified phase detector system.

With the input signal more positive than the peak detector output, the comparator turns on, forward biases D_1, and causes the integrator A_2 to integrate negatively. This negative signal is inverted by A_3 and fed back to the comparator negative input. When the integrator output magnitude reaches that of the input signal, the comparator turns off, reverse biasing D_1 and stopping the integration process. The system stabilizes to within 0.01 percent of the peak value after several cycles of the ac input.

The diode D_1 has a reverse leakage current of approximately 10 nA. It is significant that this leakage current causes the integrator to drift towards zero. The comparator senses this and corrects for it. The maximum error due to this drift, even at 100 Hz, where the time between peaks is 10 ms, is of the order of 100 mV for the parameters used in the actual system. If this diode leakage were not present and the integrator happened to drift towards a larger output value, the comparator could not correct at all.

Input dividers are required at the comparator, since a maximum of 7.0 V can be applied to its inputs. Although not precisely matched, the dividers are switched in such a way that the gain of the positive peak detector is equal to the gain of the negative peak detector [4]. In addition, the effects of comparator offset are the same for both positive and negative peak detectors so that the overall ratio of positive output peak-to-negative input peak remains accurate. After each peak read-and-hold cycle, the system is reset via a minature reed relay, which discharges the integrator feedback capacitor. Any problem due to dc offset in the ac signal source is eliminated in this system by comparing the peak-to-peak output of an amplifier under test to the peak-to-peak input.

Fig. 7 gives a simplified schematic of the phase detector system which is intended to measure the small phase shifts encountered at frequencies up to 1 kHz. The input ac test signal is applied to both the amplifier (set up as a unity-gain inverter) and one input of summer A_1. The output of the amplifier, nominally 180° out of phase with the input, is applied to the other summer input. Thus if both signals are 20 V peak-to-peak, and a phase error of θ is assumed, it follows that the output of A_1 is

$$V_0 = 10 \sin wt - 10 \sin (wt + \theta)$$
$$= 20 \cos\left(wt + \frac{\theta}{2}\right) \sin\left(-\frac{\theta}{2}\right)$$

which is a cosine wave whose peak amplitude is, for small values of θ, proportional to the phase error (approximately 0.174 V/degree). This peak value occurs midway between the zero-crossing points of the stimulus and response signals. The control logic causes the output of A_1 to be sampled on the zero-crossing of the output response signal. This technique of phase measurement assumes equal signal amplitudes. Since phase error measurements are made only at low frequencies (not greater than 1 kHz), the 580 amplifiers will have a gain of - 1.0 for this range, and so this assumption is justified.

An identical analysis applies when measuring the phase shift of multipliers. If one input is held at - 10 V, a gain of - 1.0 is provided for the ac signal applied to the other input.

The other components of the analog measurement system are a comparator, used for level sensing during RESET tests, a 500-Ω load used for output current tests, and the analog computer's digital voltmeter, which is used by the digital

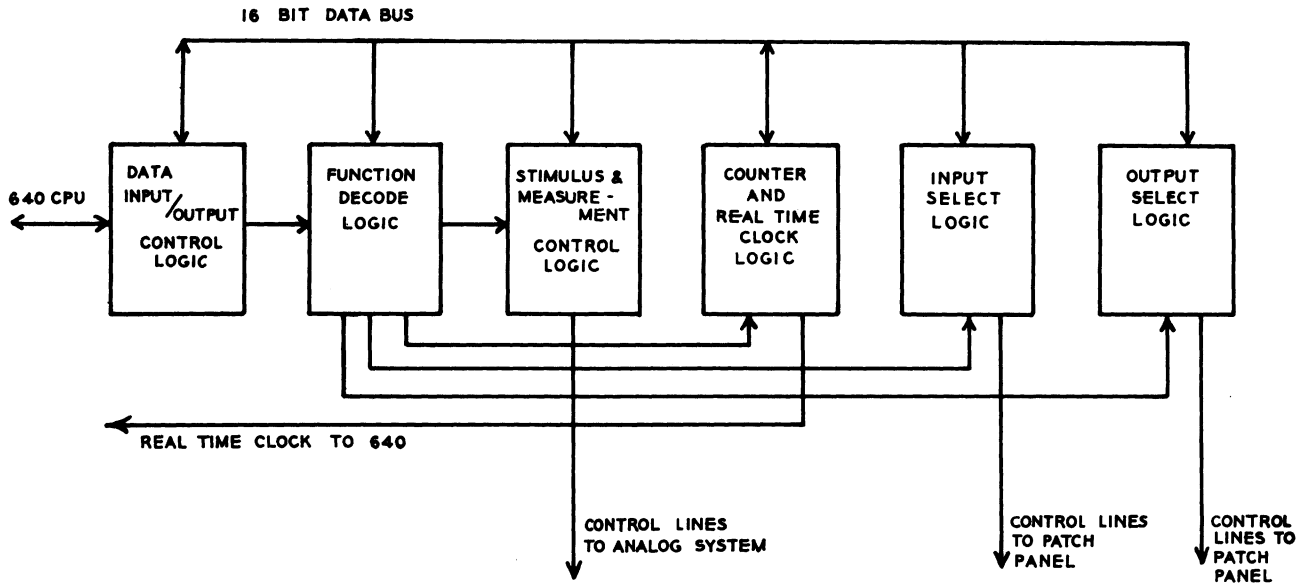

Fig. 8. Logic system organization.

computer to read in all dc signals, including the outputs of the peak detector and phase detector systems.

V. Logic System

Fig. 8 shows the organization of the digital logic system. All control is initiated through the execution of a single output instruction by the EAI 640 Digital Computer, which transfers a 16-b data word to the logic system. The most significant 8 b of the computer data word contain a "function code" which is decoded by the Function Decode Logic in order to enable the appropriate portion of the system. The least significant 8 b of the data word contain data for the particular function code.

Complete control of the stimulus and measurement systems is provided by the logic. Selected inputs can be connected to either stimulus bus, while device outputs can be selected to the response bus, under control of the digital computer. In addition, signals are generated which control the amplifier configurations, and the state of the track/store and digital/analog switch circuits. The counter and real-time clock provides timing and delay capabilities, using a basic 1-MHz crystal-controlled oscillator. Time intervals from 65 ms (1-μs resolution) up to 100 min (0.1 s resolution) can be measured for such operations as integrator and track/store reset and drift tests, and delays for relay activation and signal stabilization after switching.

VI. Software

The basic philosophy of the software system was to ensure that persons unfamiliar with the actual 640 computer hardware or ATE logic system could still write, modify, and run component test routines. In order to accomplish this, a set of Fortran callable assembler language driver routines were written to exercise the basic control of the test equipment. Once this was done, a main test program was written in Fortran. This program is run in an interactive manner from a keyboard with the operator having the ability of selecting either manual (individual component tests) or automatic (all components tested without intervention) mode and of controlling the format of the output.

VII. System Capabilities and Performance

At present, the tests which are being conducted are the following.

a) Test all servo-set potentiometers for correct setting action.

b) Test all amplifiers for balance, output current capability, phase error at 1 kHz, and frequency response to 500 kHz.

c) Test all integrators for correct functioning in all modes, drift rates in HOLD mode, and reset time in IC mode.

d) Test all track/stores for correct functioning, drift rates in STORE mode and reset time in TRACK mode.

e) Test all electronic switches for correct functioning, gain at 100 kHz and leakage current through the switch when OFF.

f) Test all multipliers for static calibration in all four quadrants, phase error at 1 kHz, and gain at 200 kHz.

g) Test all log function generators for static calibration.

h) Test all sin/cos generators for static calibration.

i) Test comparators for proper operation and switching point characteristics.

Before any tests are run, a self-test program is used to insure that the automatic test equipment is functioning correctly.

The time required to automatically test a fully expanded EAI 580 analog computer is approximately 2 h and 20 min. Of this time, 1 h and 20 min is required to perform the frequency response tests on the 64 amplifiers. This is due to the fact that, for each amplifier, four peak detections are made at eighteen different frequencies. Thus there is considerable scope for reduction of test time. For example, by reducing the number of peak detections per frequency to two, the total test time could be reduced to 1 h and 40 min.

At present, the automatic test system is being integrated into a total package which will test all portions of the hybrid system (i.e., digital peripherals, CPU and memory, interface, etc.) on a regular basis.

VIII. Conclusions

An automatic test system for the analog portion of a hybrid computation system has been described. The test system permits the analog computer to be completely dynamically tested in a much shorter time than would be required for manual testing. The techniques used in the test system are not limited to a particular analog computer. In fact, they can be applied to the testing of many types of equipment.

References

[1] J. J. Blum, *Introduction to Analog Computation*. New York: Harcourt, Brace, and Javonovich, 1968.

[2] *HOI Reference Handbook*, Electronic Associates, Inc., West Long Branch, N.J., 1970.

[3] J. E. Stuehler, "Hardware/software tradeoffs in testing," *IEEE Spectrum*, vol. 5, pp. 51-56, Dec. 1968.

[4] J. F. Ross, "An Automatic test system for analog computers," M.Sc.E. thesis, Elec. Eng. Dep., Univ. New Brunswick, Fredericton, N.B., Canada, May 1972.

Automatic Check and Calibration of Digital Voltmeters

BO MARTHINSSON, STUDENT MEMBER, IEEE, AND ERLAND MAX, STUDENT MEMBER, IEEE

Abstract—**Reliable measurement values require constant attention to the performance of the instruments. Great benefits would be achieved if the instruments had built-in fail-safe automatic check procedures. A new principle has been developed for automatic checking and calibration of a digital voltmeter. The entire instrument from the input terminals to the display is included in the check. To check the reference voltage two references are used, and they are automatically compared to each other. For each measurement value the instrument simultaneously checks itself. A simple single ramp voltmeter has been equipped with this self-checking device, and very promising results have been achieved.**

I. Introduction

IN MODERN instrumentation the role of the skilled measurement engineer is often taken over by a digital computer. Since the instruments are not constantly monitored, the risk of incorrect measurement values being used is increased.

How can incorrect measurement values be avoided? One solution is, of course, to calibrate the instruments quite often. A complete calibration of an instrument, however, demands a lot of high-precision equipment and must be carried out by a calibration laboratory. Another solution to the problem is to make the instrument capable of calibrating itself except for the necessary calibration of a simple and easily replaceable reference unit. In practice, this calibration is carried out at two points, zero and full-scale reading. Most of todays digital voltmeters are equipped with this type of calibration, but only a few have automatic calibration.

To get high dependability the instrument must, however, also be able to discover deviations from the straight line drawn through the two calibration points and deficiencies in the calibration. Thus a check circuit should be incorporated into the instrument.

There are very few instruments on the market that are equipped with a check capability. No one was found that fulfilled the following principles: 1) the automatic check should be made from the input terminals to the output display, 2) each measurement value should be checked as soon as it is obtained, and 3) the instrument should be inexpensive; no special high-quality circuits except the reference unit should be needed.

This paper will describe a check method which satisfies these principles. The automatic check operates as follows. When an input voltage has been measured, three additional check measurements are performed. These check signals are linear combinations of the input voltage, zero voltage, and reference voltage. With these four measurement values, an estimate of the measurement error is obtained. If this estimated measurement error is greater than a predetermined tolerance value, a warning signal appears.

In Section II, after a short description of a digital voltmeter in general, the check method is analyzed. Section IV describes how the automatic check procedure can be combined with an automatic calibration to make a very dependable and useful voltmeter.

II. Basic Principles of Digital Voltmeters

In general, a digital voltmeter can be described as in Fig. 1. The central part is the analog-to-digital converter A/D. Primarily, the ratio between the input voltage U and the actual reference voltage U_{ref} at the time of the measurement is measured, and to get the digital output number U_d the ratio is multiplied with the calibrated numerical value U_{refnum} of the reference voltage, e.g., established once a week or month. Thus

$$U_d = \frac{U}{U_{ref}} \cdot U_{refnum}. \quad (1)$$

Manuscript received May 8, 1973; revised July 3, 1973. This paper was presented at the 1973 Electrical and Electronic Measurement and Test Instrument Conference (EEMTIC), Ottawa, Ont., Canada, May 15-17.

The authors are with the Department of Electrical Measurements, Chalmers University of Technology, Gothenburg, Sweden.